

Modular Multilevel Converter losses model for HVdc applications

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Abstract

Multi-terminal high voltage dc (HVdc) grids can eventually become a feasible solution to transport energy to remote and/ or distant areas and its exploitation depends, among other things, on the performance of the converter terminals. Therefore, to optimize the power transmission strategy along such a grid, it is necessary to recognize the efficiency of all the converters in all points of operation, namely with the different load conditions. In this vision, the aim of this work is to provide the methodology to model the modular multilevel converter (MMC) efficiency by means of a mathematical expression that can describe, over a broad range of active and reactive power flow combinations, the power losses generated by the semiconductors. According to the presented methodology, a polynomial-based model with a reduced number of coefficients is deduced, in such a way that can be directly used for optimal power flow (OPF) studies. The accuracy of the proposed model is characterized by an absolute relative error, at the worst scenario, approximately equal to 3%.

Keywords

« HVDC converters », « AC-DC power conversion », « Losses », « Data Models »

1 Introduction

Over the past years, it is being witnessed the worldwide energy demand increase and the expansion of the transmission networks, putting at risk the security of energy supply to the consumers. Those premises are some of many foundations that are driving the research in a broad range of the electrical engineering fields, namely on the energy generation and transmission sectors. In this vision, the high-voltage dc (HVdc) transmission is being pointed as one possible key-point breakthrough.

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HVdc transmission systems have been used extensively since the middle of the twenty century for interconnecting asynchronous ac networks and to transmit bulk electrical power over long distances, adopting line commutated converters (LCC). In the late 90's the voltage source converter (VSC) solution was introduced in the HVdc field, changing the paradigm of dc transmission [1, 2]. Several VSC-HVdc-based solutions and control schemes have been proposed and implemented over three HVdc generation projects [2–4]. Currently, the fourth VSC-HVdc generation, is the modular multilevel converter (MMC) structure. It was patented in 2001 [5], and it was commercialized in 2010 in the Trans Bay project. The HVdc-based MMC has a modular realization which influences its high number of levels, requiring less ac filters than the previous VSC-HVdc solutions [3, 6]. Its modularity is achieved by the series connection of individual components called submodules (SM). Several SM power structures are found in the literature with one or more energy storage devices [7]. In opposition to the three previous VSC-HVdc generations which embraced the series connection of IGBTs, the MMC based projects have a series of connection of SM which allow to synthesize a multilevel voltage waveform at its output.

A transversal research question to the current VSC-HVdc solution is its efficiency. Depending on the SM structure there are qualitative and quantitative assessments that characterize them [7, 8]. Highlighting the half-bridge SM structure, which is until now the most efficient [9], is being investigated by several authors in nominal power conditions [10–12]. References [10] and [11] estimates the MMC generated losses at the converter nominal active/reactive power flow ratio conditions, in conjunction to a capacitor voltage ranking and selection algorithm. Reference [11] compares the converter efficiency driven by a broad range of modulation techniques, under nominal power flow conditions. On the other hand, the reference [12] determines converter losses at nominal conditions either with unity or zero power factor. However, there is a lack of information of the converter efficiency whenever it operates below its rated conditions.

Nowadays, the multi-terminal onshore and offshore dc grids schemes are a reality for power transmission [13–17]. The overall efficiency of the power transmission scheme has a relevant impact from the converter insight, whose efficiency, varies according to the load stress. Therefore, to properly introduce the converter losses into the optimal power flow (OPF) system studies, an accurate analytic calculation of the losses for an MMC must be used. As a result, the goal of this paper is to provide a methodology that can be followed to deduce a mathematical and continuous-based model that can describe the semiconductor's power losses of a grid-tied MMC. The outcome of this methodology are the coefficients that define the polynomial-based expression that can estimate the power losses produced by the semiconductors of the MMC. Moreover, the expression is characterized by a reduced number of constants and it has a straightforward application to the OPF studies.

Moreover, two expressions are deducted which describe the converter efficiency behavior under different operation modes. The first model describes the MMC efficiency when it operates within

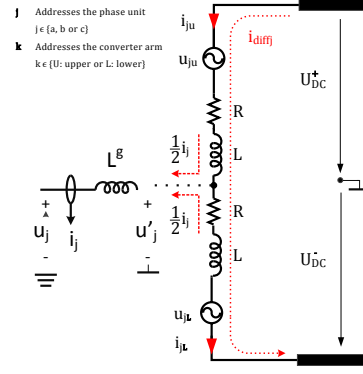
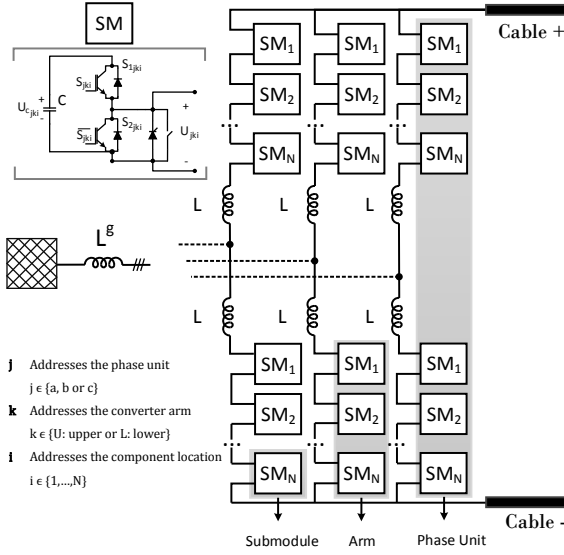


Figure 2: MMC electrical equivalent circuit (inverter Cable - mode).

Figure 1: Three-phase sketch of the modular multilevel converter.

its limits with unity power factor and its efficiency is also adjusted according to the switching frequency selected for the converter. The second part focuses on the converter efficiency when it operates, also below the nominal conditions, but exchanges active and reactive power with the electrical grid, with constant switching frequency. In Section 2 it is pointed the converter operation and its impact on the converter efficiency. The Section 3 describes the methodology adopted to estimate the converter efficiency. Later on the Section 4, it presents the inference used in getting the aforementioned models. Finally, the closing remarks are formalized in Section 5.

2 Modular Multilevel Converter

2.1 Topology

The three-phase MMC sketch is presented in Figure 1. Each phase unit is composed by two stacks of N individual low-voltage-rated power converters designated as cells or submodules (SM). The power converter is composed by a chopper and an energy storage device, typically a capacitor C. The upper (S_{1jki}) and lower (S_{2jki}) switches of the half-bridge converter are complementary closed to manage the SM states by means of the cell control signal S_{jki} . The enforcement of the control signal as $S_{jki}=1$ closes the upper switch and connects the correspondent charged capacitor $U_{c_{jki}}$ to the SM terminals U_{jki} . Forcing the control signal S_{jki} to zero, the lower switch bypasses the SM output which removes the capacitor from the arm current path and U_{jki} equals zero (1).

$$U_{jki}(t) = \begin{cases} U_{c_{jki}}(t), & \text{if } S_{jki}(t) = 1 \\ 0, & \text{if } S_{jki}(t) = 0 \end{cases} \Rightarrow U_{jki}(t) = S_{jki}(t)U_{c_{jki}}(t) \quad (1)$$

The SM states are regulated to impose particular voltages on the arm stacks u_{jk} (2). The arm

voltage varies from zero, if all the cells are bypassed, to its maximum voltage with the insertion of all the charged capacitors in the stack U_{jk}^Σ (3). The progressive change of the SM states synthesizes an exceptional arm voltage waveform. One of the design stages of the converter is the agreement between the number of the SM at the arms and the correspondent voltages. According to (3), several combinations between N and $U_{c_{jki}}$ can lead to the same voltage magnitude U_{jk}^Σ . The increase of the number of cells in the each stack N conjointly with the reduction of the capacitor's voltage leads to a higher number of voltage steps at the converter output.

$$u_{jk}(t) = \sum_{i=1}^N U_{jki}(t) = \sum_{i=1}^N S_{jki}(t) U_{c_{jki}}(t) \quad (2)$$

$$U_{jk}^\Sigma(t) = \sum_{i=1}^N U_{c_{jki}}(t) \quad (3)$$

The three MMC legs are connected in parallel on the dc side. The energy storage deviation between each leg originates the flow of electrical currents between them, which are limited by the arm inductors L . On the other hand, the ac bus of the converter is decoupled from the ac network by a transformer, modeled by its leakage reactance and then represented as an inductor L^g . The parasitic resistive components of both inductors are represented as R .

2.2 Converter Operation

In HVdc-based applications there are hundreds of submodules placed in each stack [18]. Although the number of active cells in each stack is varied to shape an ac voltage waveform, the number of active SM in each phase unit must withstand the dc voltage, due to the fact that the each converter leg is connected in parallel to the dc link. In this way, the number of active SM in each phase unit stays a relatively constant. For a grid-tied inverter, at steady-state and normal operation, the power incoming from the dc transmission line is divided equally on the three legs of the converter which globally charges the energy stored on the converter. Therefore, the arm voltages are then managed to control the grid currents i_j at the point of common coupling (PCC) and the inner differential currents i_{diff_j} in order to balance the energy storage distribution inside the converter. Adopting direction of the grid-side and the internal currents presented in the functional MMC circuit of the Figure 2, the arm currents i_{jk} are defined as:

$$\begin{cases} i_{jU}(t) = \frac{i_j(t)}{2} + i_{diff_j}(t) \\ i_{jL}(t) = -\frac{i_j(t)}{2} + i_{diff_j}(t) \end{cases} \quad (4)$$

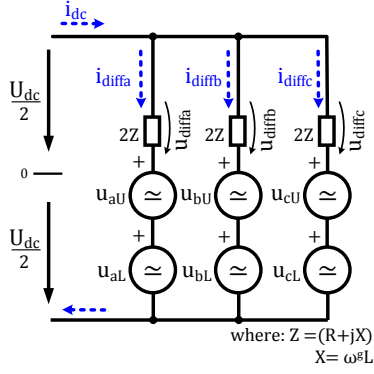


Figure 3: Internal converter dynamics representation.

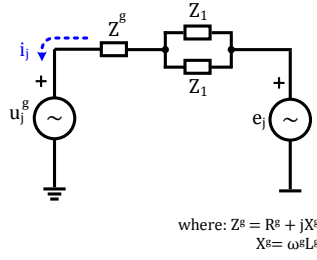


Figure 4: External converter dynamics representation.

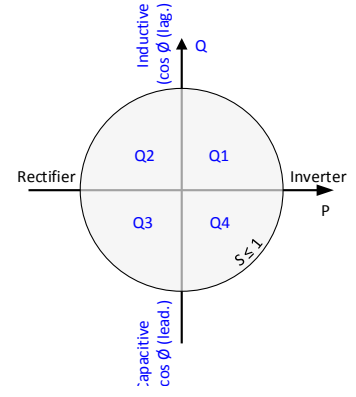


Figure 5: Four power quadrants representation.

The converter dynamics are modeled according to the KVL applied to the converter arms (5).

$$\begin{cases} U_{DC}^+ - u_{jU}(t) - Ri_{jU}(t) - L \frac{di_{jU}(t)}{dt} - u'_j(t) = 0 \\ -U_{DC}^- + u_{jL}(t) + Ri_{jL}(t) + L \frac{di_{jL}(t)}{dt} - u'_j(t) = 0 \end{cases} \quad (5)$$

where u'_j is the voltage of the mid-point between the two stacks and is given by (6).

$$u'_j = Ri_j(t) + L^g \frac{di_j(t)}{dt} + u_j^g(t) \quad (6)$$

The subtraction of the equation system (5) retrieves the dynamics of the internal currents of the converter in respect to the arm voltages as (7).

$$\begin{aligned} u_{diffj}(t) &= \underbrace{U_{DC}^+ + U_{DC}^-}_{U_{DC}} - (u_{jU}(t) + u_{jL}(t)) \\ &= 2 \left(L \frac{di_{diffj}(t)}{dt} + Ri_{diffj}(t) \right) \end{aligned} \quad (7)$$

The control of the voltage drop on the two phase unit's impedances is embraced to regulate the converter internal currents i_{diffj} , being used to cancel the energy deviation between the converter arms and legs [19]. The Figure 3 illustrates the internal current dynamics. Regulating the mean value of $(u_{jU} + u_{jL})$ handles the mean current value of the differential current i_{diff} and globally charges or discharges the energy stored on the correspondent phase unit according to the current direction [19]. Moreover, an alternate voltage drop on the two arm impedances is used to equalize the energy storage of the upper and lower arms [19].

On its turn, by adding the equation system (5), the interactions between the converter output voltage e_j and the ac grid voltage u_j^g are modeled as (8).

$$e_j(t) = \frac{-u_{jU}(t) + u_{jL}(t)}{2} = R_{eq}i_j(t) + L_{eq} \frac{di_j(t)}{dt} + u_j^g(t) \quad (8)$$

where:

$$R_{eq} = R^g + \frac{R}{2} \quad L_{eq} = L^g + \frac{L}{2} \quad (9)$$

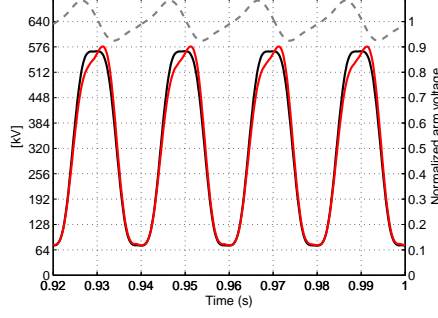


Figure 6: Arm voltage vs. its normalization.

The regulation of the converter stacks and, accordingly, the converter output voltage e_j addresses the electrical current control at PCC, as illustrated in Figure 4. The amplitude and phase of the converter output voltage establishes the active and reactive power flow between the converter and the network, over the four power quadrants defined in Figure 5. To synthesize the same line-to-line voltage at the converter output with a lower number of active SM on the stacks, the homopolar third harmonic $\text{THI}(t)$ depicted in (10) was aggregated to the converter's output voltage e_j^* [11, 20, 21].

$$\text{THI}(t) = \hat{E}_j \frac{1}{6} \cos(3\omega^g t + \phi) \quad (10)$$

Solving (7) and (8) to the arm voltages u_{jk} , is obtained the proportion of the e_j and u_{diff_j} on the arm voltages. Grid current controllers, as also the inner current controllers, respectively demand the correspondent set-points e_j^* and $u_{diff_j}^*$ being then used to determine the arm voltages reference as:

$$\begin{cases} u_{jU}^*(t) = \frac{U_{DC}(t)}{2} - e_j^*(t) - \frac{u_{diff_j}^*(t)}{2} \\ u_{jL}^*(t) = \frac{U_{DC}(t)}{2} + e_j^*(t) - \frac{u_{diff_j}^*(t)}{2} \end{cases} \quad (11)$$

Analyzing the equations (7), (8) and (11), as long as the converter is not saturated, it is noticeable that the dynamics of the ac and dc-sides of the converter are decoupled and independently controlled. The subsequent action to the definition of the stack voltage set-point u_{jk}^* is the selection of the N_{jk} cells to become active. This procedure not only follows the reference u_{jk}^* , but also maintains the energy distribution of the cells controlled and within its limits. To perform this task, the stack voltage set-point is normalized (12) and the N_{jk}^* most suitable cells (13) are selected to become active, resulting then the arm voltages illustrated in Figure 6.

$$m_{jk}^*(t) = \left(\frac{u_{jk}^*(t)}{U_{jk}^\Sigma(t)} \right) \quad (12)$$

$$N_{jk}^*(t) = \text{round}(Nm_{jk}(t)) \quad (13)$$

2.3 Voltage ripple in U_{jk}^Σ

Due to the successive change of the number of inserted capacitors in the stack N_{jk} , its equivalent capacitor C_{jk}^{eq} varies over the time (14), which, along with the arm current circulation, leads to several harmonic components of the cell's voltage sum ripple (15) [22].

$$C_{jk}^{eq}(t) = \frac{C}{N_{jk}(t)} = \frac{C}{Nm_{jk}(t)} \quad (14)$$

$$i_{jk}(t) = C_{jk}^{eq}(t) \frac{du_{jk}(t)}{dt} \iff i_{jk}(t)m_{jk}(t) = \frac{C}{N} \frac{dU_{jk}^\Sigma(t)}{dt} \quad (15)$$

Focusing on the upper stacks and replacing (4), (11) and (12) into (15) it is obtained the expression that describes the harmonic content of the cell's voltage sum and the correspondent arm operating conditions in (16). Considering that the converter is at steady-state mode and the arm's energy is equally balanced, there is no current flowing between the converter legs, and i_{diff_j} is reduced to one third of the dc transmission current. In this vision, and neglecting the parasitic resistance of the arm inductors, the expression of the voltage ripple in U_{jU}^Σ is simplified to (17).

$$\frac{dU_{jU}^\Sigma(t)}{dt} = \frac{N}{C} \underbrace{\left(\frac{i_j(t)}{2} + i_{diff_j}(t) \right)}_{i_{jU}(t)} \underbrace{\left(\frac{\frac{U_{dc}}{2} - e_j(t) - \frac{u_{diff_j}(t)}{2}}{U_{jU}^\Sigma(t)} \right)}_{m_{jU}(t)} \quad (16)$$

$$\frac{dU_{jU}^\Sigma(t)}{dt} = \frac{N}{C} \left(\frac{i_j(t)}{2} + \frac{I_{dc}(t)}{3} \right) \left(\frac{\frac{U_{dc}}{2} - e_j(t)}{U_{jU}^\Sigma(t)} \right) \quad (17)$$

The eq. (17) shows that the magnitude and phase of $i_j(t)$ and $e_j(t)$, namely the magnitude of the active and reactive power flow at PCC, has a significant impact on the harmonic content and its amplitudes on U_{jk}^Σ , and accordingly on the individual capacitor voltages $U_{c_{jki}}$. As a consequence, the power flow conditions of the MMC impacts the voltage ripple of its capacitors and, consequently, the average switching frequency of the semiconductors will be also affected, as explained in the Section 2.4.

2.4 Cell selection

As the converter is characterized by the series connection of independent SMs, several combinations of their states can be used to build the demanded arm voltages $u_{jk}^*(t)$. By managing the state of the i^{th} cell S_{jki} (defined in the Figure 1) the current flow through the capacitor have a direct impact on its state of the charge (SoC). Besides the selection of a target number of capacitors to be inserted N_{jk}^* , the individual voltages of the cells must be monitored to maintain them balanced

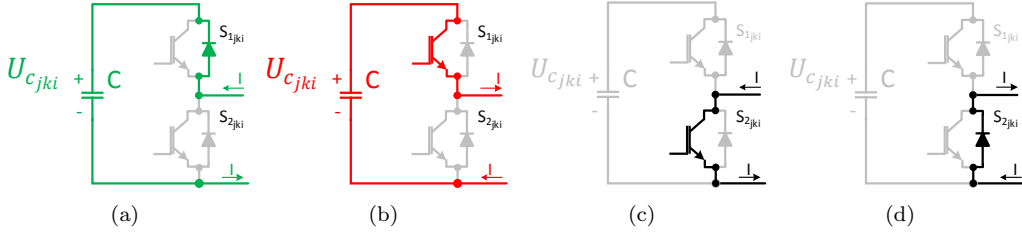


Figure 7: States of an half-bridge-based cell: (a) the capacitor is charging, (b) the capacitor is discharging and the submodule is bypassed with (c) positive and (d) negative current in the arm.

and/ or within the limits [23]. Hence, the selective control of the SMs must be done accordingly to the stack operating point and their individual voltages [6]. First, the voltages of the cells $U_{c_{jki}}$ are ranked in an ascending or descending order, either the arm current is positive or negative, and the correspondent position of the capacitors are recorded in a list L [6, 23]. Then, the first N_{jk}^* cells of the computed list, which retrieve smallest error to the u_{jk}^* , are elected to be inserted in the series chain, whereas the remaining $(N - N_{jk}^*)$ cells are short-circuited. Under these circumstances, whenever the stack current is positive (negative) and according to the sorted list, the N_{jk}^* cells with the lowest (highest) voltages are inserted in the chain, which boosts (lowers) their voltages.

Several selective control algorithms of the cells have been proposed in the literature with different characteristics [6, 23–25]. The reference [11] presents and experimentally validates the selection strategy named CTBsort which balances the energy of the stack cells and maintains the correspondent voltages below the imposed limits. Due to its promising performance, the CTBsort cell selection method was adopted for this study. In this method, as long as the capacitor voltages $U_{c_{jki}}$ remain inside the voltage range defined by V_{max} and V_{min} (18), the sorted list L of capacitor voltages is not updated [11].

$$\begin{cases} V_{max} = (1 + \delta)U_{nom} \\ V_{min} = (1 - \delta)U_{nom} \end{cases} \quad (18)$$

where δ is a constant that defines the voltage band around the capacitor's nominal voltage U_{nom} .

Once at least one cell hits the voltage limits defined by V_{max} and V_{min} , the ranking list of the correspondent stack is updated in the ascending (descending) order in case that the arm current is positive (negative). As a consequence, once the capacitors that have their voltage limits violated¹, they will be forced to swap [11]. As the voltage range defined by δ is reduced, more often the capacitor voltages hit their limits and, as a result, the cells are more often replaced. Then, it is concluded that the voltage range defined by δ directly impacts the MMC switching frequency.

3 Semiconductor's power losses model deduction

According to the MMC nature, the fact of being composed of individual elements connected in series, the number of active cells N_{jk} in a given instant depends on the reference created by

¹The voltage limits V_{max} and V_{min} are defined in accordance with δ (18).

the converter control method N_{jk}^* . Thus, it can be said that the number of devices in series at a particular time does not depend on cell selection method, as long as, the adopted method is capable to insert the required number of SMs in the chain (19). So, if at each particular operating point (19) is verified, the number of semiconductors in the on-state mode will remain equal for any strategy adopted to select the cells, quantifying then the same on-state losses.

$$N_{jk}^*(t) = N_{jk}(t) \quad (19)$$

The cell selection methods solely impact on the energy distribution among the capacitors in the jk arm and hence on the converter's average switching frequency, as depicted in Figure 8. Focusing on the CTBsort method discussed in the previous section, from the variation of the capacitor voltage limits δ and the corresponding power conditions of the MMC, it were deduced two mathematical models representative of the semiconductor losses. The first model is characterized by the semiconductor's power losses, whenever the MMC is exchanging only active power with the electrical grid (unity power factor). Then, the referred model is capable to predict the semiconductor's model as a function of the active power flow and the switching frequency of the converter. Consequently, the second model is characterized by estimating the semiconductor's power losses whenever the converter is exchanging active and reactive power with the electrical grid, but with a fixed switching frequency. On the MMC-HVdc-based applications, typically the average switching frequency varies around 150 Hz due to the semiconductor limits and practical limitations [7, 20, 26, 27]. Therefore, as it will be reinforced later, the capacitor voltage limits were varied, by means of δ , in order to achieve this fixed commutation ratio. Depending on the MMC operating conditions, the proper losses model should be selected.

The procedure used to deduct a generic expression that can represent the converter losses was structured in three distinct stages. The first stage is characterized by simulating and recording the outcome data, considering the converter operation with ideal switches inside the cells, further explained in Section 3.1. Consequently, the acknowledged data was used to calculate the semiconductors generated losses in offline mode, which is discussed in Section 3.2. Finally, the inference of the mathematical model is accomplished in Section 4.

3.1 Simulation data extraction

The point-to-point HVdc transmission line of the INELFE project [28, 29], illustrated in Figure 9, was embraced in this work to assess the MMC efficiency. The two HVdc-link terminals have the same characteristics presented in the table 1, however, differently controlled. The MMC-1 terminal was controlled as a current source which injects (absorbs) into (from) the dc transmission line a constant power, according to the pre-defined reference P_{MMC-1}^* . In its turn, the MMC 2 manages the active power flow at PCC to guarantee the voltage at the dc transmission line equal

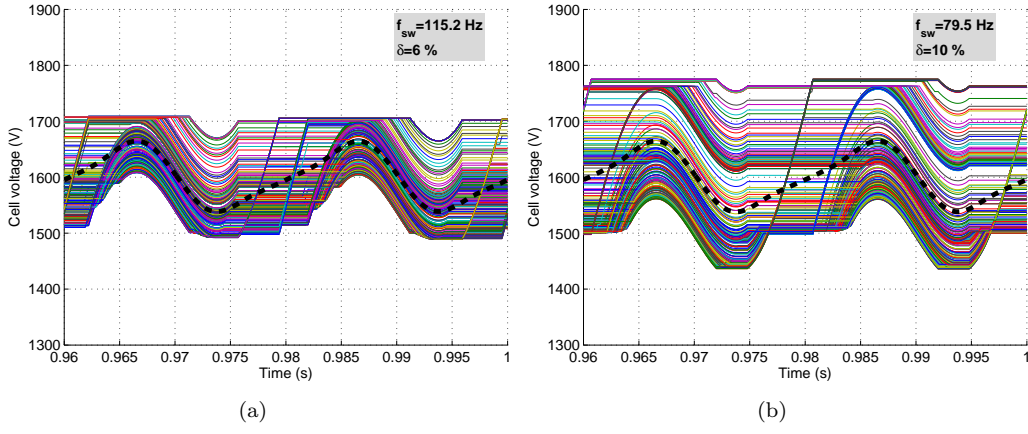


Figure 8: The capacitor voltages of one stack for a tolerance band of: (a) 6% and (b) 10%.

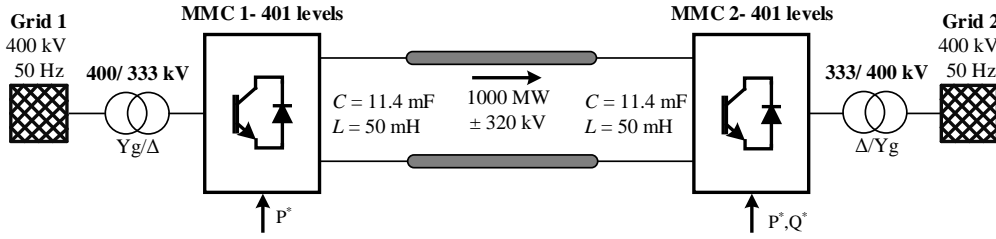


Figure 9: INELFE MMC-HVdc transmission system.

to 640 kV, as well as, the nominal energy storage on the converter stacks. Moreover, MMC-2 is able to control the reactive power that flows between the converter and the network 2, as a consequence of the desired set-point Q_{MMC-2}^* . By handling the active and reactive power flow references in both HVdc terminals with the control scheme presented in [19], the efficiency of the MMC-2 was analyzed in two independent situations. First, the set point Q_{MMC-2}^* was left equal to zero, whereas P_{MMC-1}^* and δ was being changed, further detailed in section 3.1.1. On the next case study, explained in section 3.1.2, the voltage limits of the sorting algorithm were varied in order to find, for each combination of P_{MMC-1}^* and Q_{MMC-2}^* , the average switching frequency of 150 Hz, as previously argued.

3.1.1 Unity power factor condition

In order to obtain the converter's efficiency whenever it operates with unity power factor ($Q_{MMC-2}^* = 0$ Mvar) and also below its limits ($S \leq 1$ pu), the active power flow reference on the MMC-1 terminal P_{MMC-1}^* was varied from 1 to 0.1 pu. Then, for each particular steady-state scenario $P_{MMC-1}^* = P_{MMC-2}^*$, the voltage limits of the capacitor voltages δ were varied from 5% to 15%. For the same active power flow condition, the fact of varying the tolerance band voltage of the capacitors subsequently changes the average switching frequency of the semiconductors.

The procedure adopted to extract the simulation data for the unity power factor condition is illustrated in the Figure 10 and the Algorithm 1. For each particular combination of (P_{MMC-1}^* , $Q_{MMC-2}^* = 0$, δ), the data resultant from the simulation was recorded in an individual file to be processed later. The simulation data recorded by the algorithm 1 is based on the system parameters

Table 1: Circuit Parameters used in simulation

Parameters	Notation	Value
Number of submodules/arm	N	400
Rated apparent power	S	1.0 GVA
Line voltage	U_{LL}	333 kV
dc-bus voltage	U_{dc}	± 320 kV
Cell capacitance (35 kJ/MVA)	C	11.4 mF
Nominal submodule voltage	U_{nom}	1.6 kV
Rated submodule voltage	U_{SM}^R	4.5 kV
Arm inductance	L_{arm}	50 mH
Grid Inductance	L_{grid}	50 mH
Parasitic resistance of the inductors	R	0.1 Ω
Sampling frequency	f_s	10 kHz
Converter model	Data equivalent model (Type 4) [30–34]	
Arm voltage modulation	Nearest level Modulation [35]	
Zero sequence signal	Third harmonic injection	
Cell selection method	CTBsort [23]	
IGBT device model	ABB 5SNA2000K450300	

that feed the "MMC model & control" stage, as well as, the methodology followed to modulate the voltages across the converter arms (nature of the ZSS and selective control of the capacitors).

3.1.2 Fixed switching frequency

Due to the non-linear behavior between the power flow conditions, capacitor's voltage ripple and the average switching frequency of the cells, it was decided to study the efficiency of the converter over several combinations of $\{P_{MMC-1}, Q_{MMC-1}\}$ ($S \leq 1$), but with fixed switching frequency. To accomplish this task, it was implemented the algorithm illustrated in the Figure 11, which is detailed in the Algorithm 2. As the algorithm shows, per each combination of active and reactive power flow conditions (P_{MMC-1}, Q_{MMC-2}), the SM's voltage range was incremented/decremented until it was found the value of δ that retrieved the average switching frequency² of the 6N cells within the interval [149, 151] Hz.

Once the suitable value of f_{sw} was found, a new data file was created with the simulation data, to be later processed. The simulation data recorded by the algorithm 2 is based on the system parameters that feed the "MMC model & control" stage, the switching frequency f_{search} intended, as well as, the methodology followed to modulate the voltages across the converter arms (nature of the ZSS and selective control of the capacitors).

3.2 Quantification of the semiconductors power losses

Several methods to estimate the semiconductor' power losses have been proposed [36–40]. The methodology followed was proposed by the MMC's manufacturer Siemens AG [36], and it is being widely used since then [12, 25, 26, 41]. The method embraced estimate the semiconductor's power losses in respect to the simulation results and the characteristics of a particular semiconductor model [36].

The quantification of the losses generated is dependent on the semiconductor device adopted. Considering the HVdc transmission link presented, the average voltage of the cells is 1.6kV and

²In this work, the average switching frequency of the cells was determined by means of the semiconductor's gating signals in respect to the last 5 fundamental cycles of the grid frequency.

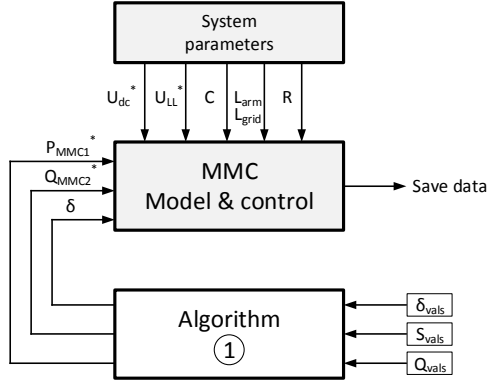


Figure 10: Block diagram of the algorithm 1.

Algorithm 1: MMC-2 operation
 $S \leq 1$, $\cos\phi=1$, $5\% \leq \delta \leq 15\%$

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1: procedure GET FILES 1
2:    $S_{nom} \leftarrow 1.0$  GVA
3:    $U_{nom} \leftarrow 1.6$  kV
4:    $S_{vals} \leftarrow [1 : -0.1 : 0.1]$  pu
5:    $Q_{vals} \leftarrow 0$  pu
6:    $\delta_{vals} \leftarrow [0.15 : -0.005 : 0.05]$  pu
7:   for  $i=1:\text{length}(S_{vals})$  do
8:     for  $j=1:\text{length}(\delta_{vals})$  do
9:       Simulate MMC-HVDC transmission with:
10:       $P_{MMC-1}^* \leftarrow \sqrt{(S_{vals}(i)S_{nom})^2 - Q_{vals}}$ 
11:       $Q_{MMC-2}^* \leftarrow Q_{vals}$ 
12:       $v_{max} \leftarrow (1 + \delta_{vals}(j)) U_{nom}$ 
13:       $v_{min} \leftarrow (1 - \delta_{vals}(j)) U_{nom}$ 
14:      Create file and save results
15:    end for
16:  end for
17: end procedure

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this value fluctuates accordingly with the flowing power ($\approx \pm 10\%$ for nominal power and $\cos\phi=1$). In case of a failure occurrence in a particular cell and consequently bypassed by a contactor, the energy that was being stored is divided by the remaining cells of the correspondent stack [42]. In this vision, and to ensure the converter operation with faulted devices, the authors strongly believe that the semiconductors must be overrated, although they are operated with lower blocking voltages in normal operating conditions. Therefore, the state of the art semiconductor model ABB-5SNA2000K450300 (4.5kV / 2kA device) seems to be a viable option to quantify the losses generated by the MMC-2 case study [43].

3.2.1 On-state losses

The conducting losses of the semiconductors are affected by several phenomenons as the device's junction temperature (T_j), the voltage drop at the devices terminals (IGBTs: $U_{CE_{sat}}$ / diodes U_F), the operating currents (IGBTs: i_{CE} / diodes i_F) and, in case of IGBTs, the driver circuitry voltage (U_g). The average on-state losses of the IGBTs (P_T^{con}) and the diodes (P_D^{con}) over a grid period ($[t_s, T_s]$) are given by (20) and (21) respectively [36].

$$P_T^{con} = \frac{1}{T_{ss}} \int_{t_s}^{t_s+T_{ss}} i_{CE}(t) U_{CE}^{[U_g, T_j]}(i_{CE}(t)) dt \quad (20)$$

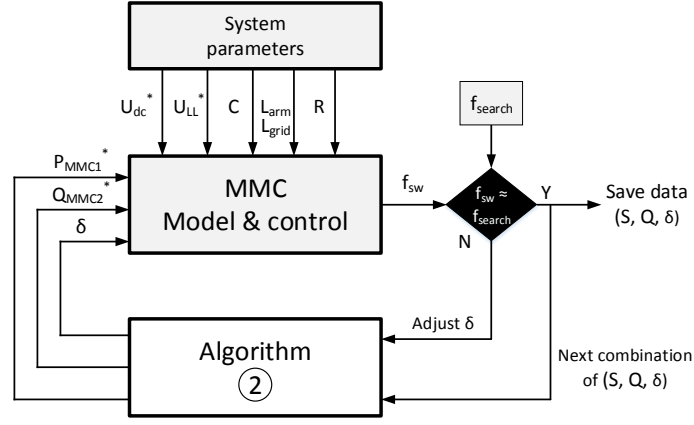


Figure 11: Block diagram of the algorithm 2.

Algorithm 2: MMC-2 operation
 $S \leq 1, \cos\phi \leq 1, f_{sw} \approx 150$ Hz

```

1: procedure GET FILES 2
2:    $S_{nom} \leftarrow 1$  GVA
3:    $U_{nom} \leftarrow 1.6$  kV
4:    $f_{search} \leftarrow 150$  Hz
5:    $S_{vals} \leftarrow [1 : -0.1 : 0.1]$  pu
6:    $P_{vals} \leftarrow [1 : -0.1 : 0.1]$  pu
7:    $\delta_{vals} \leftarrow [0.001 : 0.001 : 0.2]$  pu
8:   for  $i=1:\text{length}(S_{vals})$  do
9:     for  $j=1:\text{length}(P_{vals})$  do
10:       $S^* \leftarrow S_{vals}(i)S_{nom}$ 
11:       $P_{MMC-1}^* \leftarrow P_{vals}(j)S^*$ 
12:       $Q_{MMC-2}^* \leftarrow \sqrt{(S^*)^2 - (P_{MMC-1}^*)^2}$ 
13:      for  $k=1:\text{length}(\delta_{vals})$  do
14:        Simulate MMC-HVDC with:
15:         $(P_{MMC-1}^*, Q_{MMC-2}^*)$ 
16:         $v_{max} \leftarrow (1 + \delta_{vals}(k))U_{nom}$ 
17:         $v_{min} \leftarrow (1 - \delta_{vals}(k))U_{nom}$ 
18:        Analysis Post simulation ( $k$ ):
19:         $f_{sw} \leftarrow \text{Calculate avg. } f_{sw}$ 
20:        if  $f_{sw}(k) \in [f_{search} \pm 1]$  then
21:          Save  $\delta_{vals}(k)$ 
22:          Save simulated data in new file
23:          Proceed to next  $j$ 
24:        end if
25:      end for
26:      if NOT (find( $f_{sw}(k) \in [f_{search} \pm 1]$ )) then
27:        Save  $\delta_{vals}(k)$  w/ closest  $f_{sw}(k)$ 
28:      end if
29:    end for
30:  end for
31: end procedure

```

$$P_D^{con} = \frac{1}{T_{ss}} \int_{t_s}^{t_s+T_{ss}} i_F(t) U_F^{[T_j]}(i_F(t)) dt \quad (21)$$

The oscillation of the junction temperatures over the different operating conditions and the voltage amplitude variation on the gating circuitry were not considered ($T_j \approx 125^\circ\text{C} / U_g = 15\text{V}$). The non linear relation between IGBT's saturation voltage and the diode's forward voltage with the correspondent flowing currents, was fitted from the manufacturer component data (22), and illustrated in Figure 12(a).

$$U(i) = a + b i^c \Rightarrow \begin{cases} U_{ce_{sat}}(i_{CE}) = 0.568 + 0.02497 i_{CE}^{0.6267} \\ U_F(i_F) = 0.313 + 0.08916 i_F^{0.414} \end{cases} \quad (\text{V}) \quad (22)$$

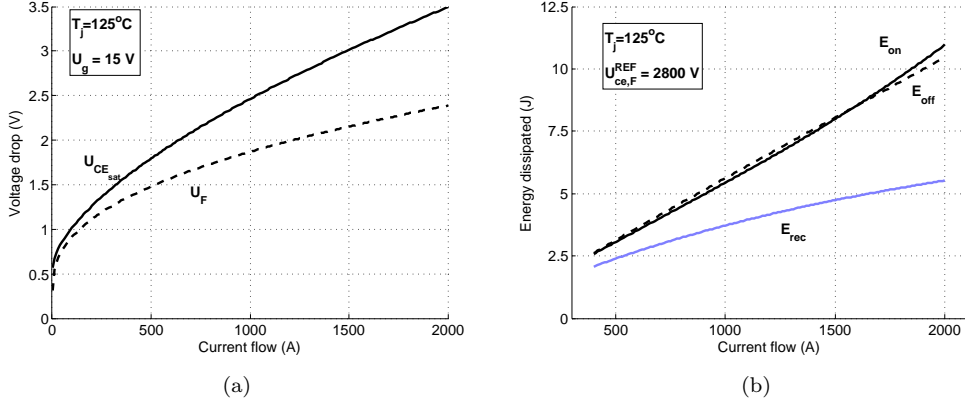


Figure 12: ABB-5SNA2000K450300 IGBT model: (a) on-state voltage droop and (b) energy lost in commutation event.

3.2.2 Switching losses

During a switching event of a semiconductor, due to its non-zero time interval, some energy is dissipated. The required time that the semiconductors need to commute has a nonlinear relation with the electrical current that is flowing on the correspondent instant. For the presented device, its characteristics were obtained from the component's data-sheet (23), and illustrated in Figure 12(b).

$$E(i) = a + b i + c i^2 + d i^3 \Rightarrow \begin{cases} E_{on}^{U_{CE}=2.8kV}(i_{CE}) = (3.527e-10)i_{CE}^3 - (7.152e-7)i_{CE}^2 + (5.216e-3)i_{CE} + 0.5816 \\ E_{off}^{U_{CE}=2.8kV}(i_{CE}) = (7.237e-11)i_{CE}^3 - (3.473e-7)i_{CE}^2 + (5.383e-3)i_{CE} + 0.5118 \\ E_{rec}^{U_F=2.8kV}(i_{CE}) = (1.231e-10)i_{CE}^3 - (1.008e-6)i_{CE}^2 + (3.965e-3)i_{CE} + 0.6427 \end{cases} \quad (J) \quad (23)$$

At each commutation event, the energy lost on the correspondent semiconductor is estimated accordingly to the switched current as (23) and linearly corrected according to the voltage at the device's terminals as (24) [36].

$$\begin{aligned} P_{onT} &= \frac{1}{T_{SS}} \sum_{\beta} \frac{U_{CE}(t_{\beta})}{U_{CE}^{REF}} E_{onT}^{[T_j]}(i_{CE}(t_{\beta})) \\ P_{offT} &= \frac{1}{T_{SS}} \sum_{\gamma} \frac{U_{CE}(t_{\gamma})}{U_{CE}^{REF}} E_{offT}^{[T_j]}(i_{CE}(t_{\gamma})) \\ P_{recD} &= \frac{1}{T_{SS}} \sum_{\kappa} \frac{U_F(t_{\kappa})}{U_{FREF}} E_{recD}^{[T_j]}(i_F(t_{\kappa})) \end{aligned} \quad (24)$$

where the $i_{CE}(t_{\beta})/i_{CE}(t_{\gamma})$ are the switched currents and $U_{CE}(t_{\beta})/U_{CE}(t_{\gamma})$ are the voltages at the IGBT terminals at the β/γ triggering/blocking events.

4 MMC generated losses model

The procedure presented to deduct an expression that defines the semiconductor's losses model of the converter is addressed in section 4.1 for the unity power factor operation and section 4.2 for the fixed switching frequency operation.

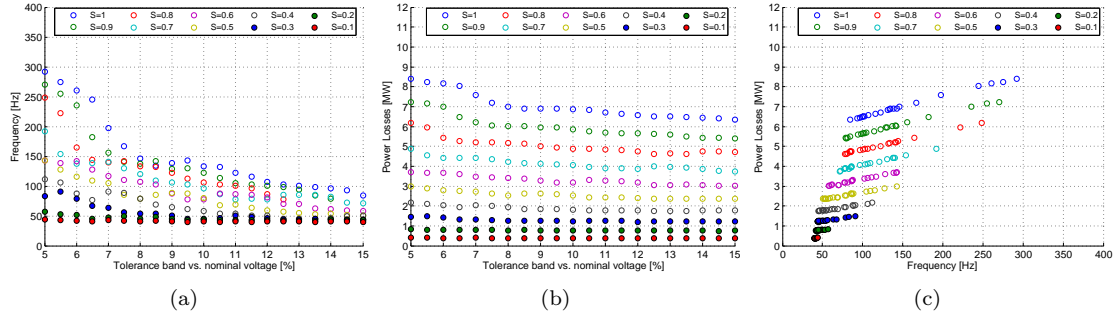


Figure 13: MMC operation with the unity power factor in inverter mode: (a) SM average switching frequency, (b) total losses - P_{loss} and (c) P_{loss} vs. average switching frequency.

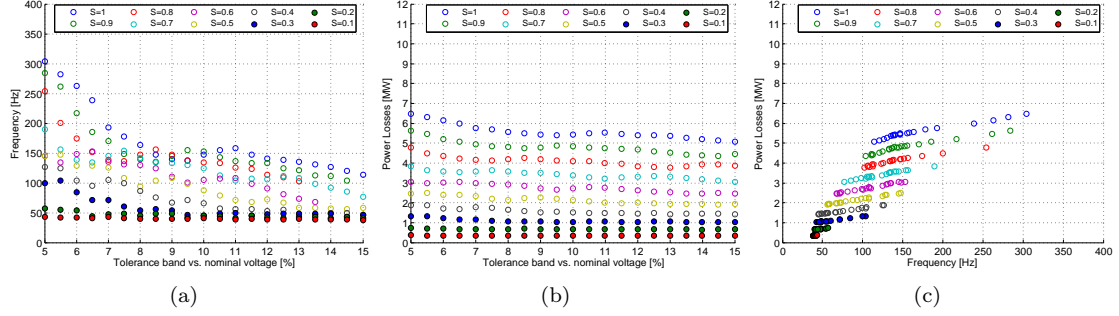


Figure 14: MMC operation with the unity power factor in rectifier mode: (a) SM average switching frequency, (b) total losses - P_{loss} and (c) P_{loss} vs. average switching frequency.

4.1 MMC efficiency - Unity power factor condition

After executing the Algorithm 1 and computing the semiconductors generated losses from its outcome data, the converter losses in respect to the active power flow (unity power factor) and the average SM switching frequency emerged and are illustrated in Figure 13 and 14 for the inverter and rectifier operation modes, respectively.

First should be emphasized that at steady-state service the SMs are globally characterized by its reduced switching frequency. For the $P > 0.5$ pu, as the trend of Figure 14 evidences, if the voltage range of the cells is increased, the average switching frequency of the switches will be further reduced. There is a trade-off between the maximum voltage allowed on the SMs and the switching frequency which is not explored in this work. However the maximum voltage allowed of 15% in this study is considered to be an acceptable and realistic value. Whenever the converter stress is below 0.2 pu, the cell selection algorithm has residual impact on the switching frequency and therefore on the generated losses, being nearly constant.

The combination between the SMs average switching frequency f_{sw} and the semiconductor's losses P_{loss} of Figure 13(c) and Figure 14(c) eliminates the dependency of the capacitor's voltage limits which is a relevant procedure to extract a generic expression capable to define the converter efficiency without the intrinsic details of the cell selection method. Re-drawing the rectifier mode results of the Figure 14(c) in the given Figure 15, by means of the yellow circles emphasized, it is possible to find a relation between the semiconductor power losses vs the average switching frequency (yellow circles for $P = 1$ pu) in the Figure 15(a), as well as, the semiconductor power

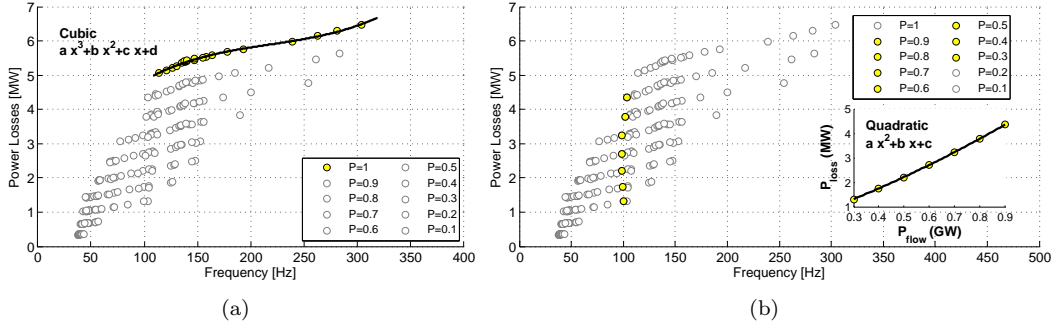


Figure 15: Illustration of the relation: (a) P_{loss} vs. f_{sw} ($P = 1$ pu) and (b) P_{loss} vs. P_{flow} ($f_{sw} = 100$ Hz).

losses vs active power flow (yellow circles for $f_{sw} = 100$ Hz) in the Figure 15(b). These two individual relations were used to deduce the mathematical model $P_{loss}(f_{sw}, P_{flow})$, in such a way that depending on the combination of (f_{sw}, P_{flow}) used, the semiconductor losses estimation is obtained.

Inasmuch as the grid power flow is 1 GW, as also for other scenarios, according to Fig. 15(a), the P_{loss} vs f_{sw} data can be comparable to a cubic progression. Likewise, fixing the SMs switching frequency to 100 Hz, as illustrated in Fig. 15(b), the converter total losses can be resembled in a quadratic form with the flowing power. Assuming those relations as the most accurate, the generated losses of the MMC can be predicted according to the generic expression (25), either resumed to a third order polynomial relation if P_{flow} is remained constant or to a second-order polynomial for a particular f_{sw} value.

$$\begin{aligned}
 P_{loss}(f_{sw}, P_{flow}) = & (a_1 P_{flow}^2 + a_2 P_{flow} + a_3) f_{sw}^3 \\
 & + (b_1 P_{flow}^2 + b_2 P_{flow} + b_3) f_{sw}^2 \\
 & + (c_1 P_{flow}^2 + c_2 P_{flow} + c_3) f_{sw} \\
 & + (d_1 P_{flow}^2 + d_2 P_{flow} + d_3)
 \end{aligned} \tag{25}$$

The Levenberg-Marquardt optimization algorithm was used to determine the values of the coefficients $(a_\gamma, b_\gamma, c_\gamma, d_\gamma)$ ($\gamma \in \{1, 2, 3\}$) that minimizes the sum of absolute deviations (LAD) (26) between the $P_{loss}(f_{sw}, P_{flow})$ model (25) and the data of Figures 13(c) and 14(c) [44]. The parameters found are presented in table 2. Moreover, the matching models for the inverter and rectifier modes are illustrated in Figure 16 and 17 respectively.

$$LAD = \sum_{i=1}^{N_{samples}} |P_{loss}^i - data^i| \tag{26}$$

As illustrated, the resultant model $P_{loss}(f_{sw}, P_{flow})$ has a good accuracy on the corresponding domain, in which the presented parameters were optimized. For sake of clarity and according to the proposed model, if the converter is injecting 1 GW in the ac grid and the capacitors are being

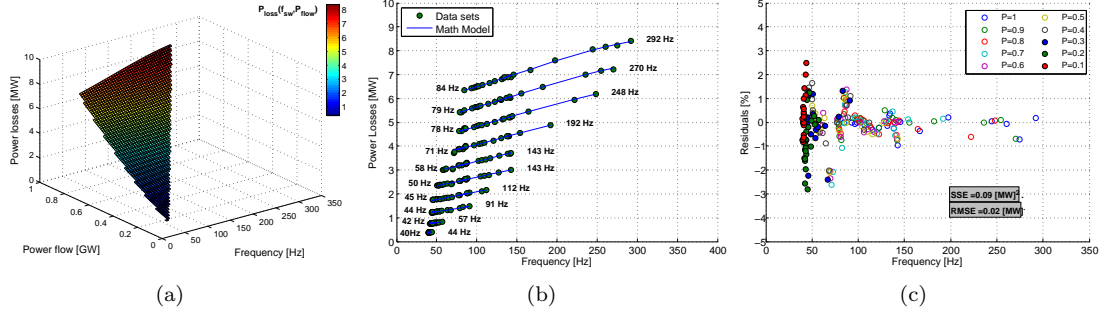


Figure 16: (a) Mathematical model of the generated losses by the MMC (unity power factor in inverter mode); (b) $P_{loss}(f_{sw}, P_{flow})$ vs simulated data and model's domain; (c) relative error.

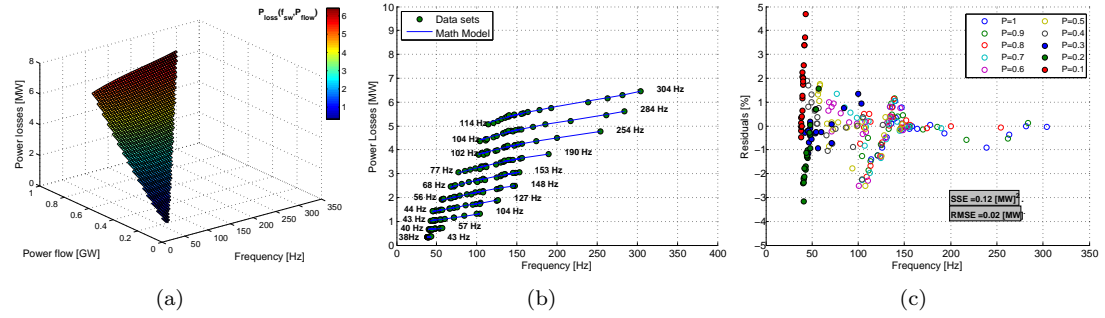


Figure 17: (a) Mathematical model of the generated losses by the MMC (unity power factor in rectifier mode); (b) $P_{loss}(f_{sw}, P_{flow})$ vs simulated data and model's domain; (c) relative error.

Parameters	Inverter Mode		Rectifier Mode	
		[pu]		[pu]
$P_{loss}(f_{sw}, P_{flow})$ model	a_1	-1.681e-11	-2.386e-10	
	a_2	-2.000e-10	6.915e-10	
	a_3	1.071e-10	-3.056e-10	
	b_1	7.150e-8	4.869e-8	
	b_2	-6.982e-10	-2.538e-7	
	b_3	-1.880e-8	1.050e-7	
	c_1	-1.988e-5	1.734e-6	
	c_2	2.107e-5	3.547e-4	
	c_3	1.957e-6	-8.944e-7	
	d_1	3.714e-3	8.379e-4	
$(S_{base}=1 \text{ GVA})$	d_2	2.045e-3	1.902e-3	
	d_3	6.798e-6	2.476e-4	

Table 2: Mathematical losses model of the converter under unity power factor conditions.

rotated with a 200 Hz cadence (see Figure 16(b)), in respect to the base value depicted in the table ($S_{base} = 1$ GVA), the power losses estimation is given by (27).

$$\left\{ \begin{array}{l} f_{sw} = 200 \text{ Hz} \\ P_{flow}^{pu} = \frac{P_{flow}}{S_{base}} = 1 \text{ pu} \end{array} \right. \Rightarrow \left\{ \begin{array}{l} P_{loss}(f_{sw}, P_{flow}) = (a_1(1)^2 + a_2(1) + a_3) 200^3 \\ \quad + (b_1(1)^2 + b_2(1) + b_3) 200^2 \\ \quad + (c_1(1)^2 + c_2(1) + c_3) 200 \\ \quad + (d_1(1)^2 + d_2(1) + d_3) \\ \quad = 0.0076 \text{ pu} \end{array} \right. \quad (27)$$

In this view, on the presented operating conditions, the mathematical model estimates that the MMC semiconductor's are dissipating 7.6 MW/0.0076 pu of power losses, which is corroborated in the Figure 16(b).

Generally, the absolute relative error is below 3%, however, for $P = 0.1$ pu (rectifier mode), the model retrieves residual values up to 5%. This occurs because there is a slightly offset between the model and the corresponding data set. Under these circumstances, the converter dissipates ≈ 450 kW and, if the model conceives a 5% deviation, has a residual impact on the final estimation ≈ 23 kW, which is acceptable.

4.2 MMC efficiency - Four P/Q power quadrants

Once implemented the algorithm Algorithm 2, and found the δ values which, for each combination of active and reactive power, retrieves the SMs average switching frequency of 150 Hz, the semiconductor losses were estimated. The MMC losses over the four $\{P, Q\}$ quadrants are shown in Figure 18. The left-sided graphs show the average switching frequency (≈ 150 Hz) and the capacitor's voltage range for each apparent power flow conditions (S in GVA) of the converter (represented in different colors). As the apparent power magnitude is reduced, the correspondent voltage ranges are becoming more concentrated around a particular δ point. On the second axis, are presented the generated losses in respect to the apparent power magnitude for different $\{P, Q\}$ combinations. For the same S , the fact that the active power is being changed means that the reactive power is being appropriately modified to equalize the referred the apparent power flow conditions. As the electrical current amplitude is reduced, the stress of the semiconductor is also scaled down, which dissipates less energy over the time. Furthermore, the MMC operation in the rectifier mode, characterized by the quadrants two and three, is more efficient than the inverter mode. This occurs due to the fact that the average number of conducting diodes over a grid period is larger than the IGBTs, and the non-controllable devices have a lower on-state voltage, which generates less losses.

The aforementioned methodology to deduct either the generic expression, as well as, its parameters to describe the losses model P_{loss} in respect to the combination ($S_{flow}, P_{flow}, f_{sw} \approx 150$

Hz) was again carried out. The power losses retrieved by the MMC on the power quadrant 2 that is illustrated in the Figure 18(b) were reconsidered in the Figure 19. Then, it was emphasized by means of the yellow circles the relation between the semiconductor power losses vs active power flow (yellow circles for $S_{flow} = 1$ GVA) in the Figure 19(a), as well as, the semiconductor power losses vs apparent power flow (yellow circles for $P_{flow} = 0.1$ GW) in the Figure 19(b). These two individual relations were used to deduce the mathematical model $P_{loss}(S_{flow}, P_{flow})$ over the four power quadrants of operation. Further, as the Figure 19(a) illustrates, for the constant value of S_{flow} presented, the losses retrieved by the $\{P, Q\}$ ratio is efficiently modeled as a cubic expression. In opposition, as shown in the Figure 19(a), for the same active power flow of 0.1 GW, the semiconductor power losses vs. the apparent power flow $P_{loss}(S_{flow})$ is competently modeled as a quadratic expression. Thereby, the $P_{loss}(S_{flow}, P_{flow})$ outcome is depicted as:

$$\begin{aligned}
P_{loss}(S_{flow}, P_{flow}) = & (a_1 S_{flow}^2 + a_2 S_{flow} + a_3) P_{flow}^3 \\
& + (b_1 S_{flow}^2 + b_2 S_{flow} + b_3) P_{flow}^2 \\
& + (c_1 S_{flow}^2 + c_2 S_{flow} + c_3) P_{flow} \\
& + (d_1 S_{flow}^2 + d_2 S_{flow} + d_3)
\end{aligned} \tag{28}$$

The Levenberg-Marquardt optimization algorithm was again used to determine the values of the coefficients $(a_\gamma, b_\gamma, c_\gamma, d_\gamma)$ ($\gamma \in \{1, 2, 3\}$) which best characterizes the MMC efficiency over the four power quadrants [44]. According to the model formulation, logically, the independent variables P and S have intrinsic limits which validates the conferred model, such as:

- S_{flow} must be within the $[0.1, \dots, 1]$ GVA ($S'_{flow} \in [0.1, \dots, 1]$ pu.);
- The P_{flow} must be inward the interval defined by $[0.1 S'_{flow}, \dots, S'_{flow}]$ GW. Therefore $P_{flow} \leq S_{flow}$ and $P_{flow} \geq 0.1 S_{flow}$.

The clusters of coefficients for the four power quadrants (Q1, Q2, Q3 and Q4), in order to be directly used on the OPF studies, they were transformed in the per-unit *pu* system and they are presented in the Table 3. The 150 Hz-based semiconductor's power loss models were deduced over the four power quadrants and they are respectively illustrated in the Figures 20(a), 21(a), 22(a) and 23(a). It is worth reinforcing that the model's coefficients $(a_\gamma, b_\gamma, c_\gamma, d_\gamma)$ were optimized for the previously mentioned domain defined as $(0.1 \leq S \leq 1)$ GVA and $(0.1 S \leq P \leq S)$ GW. Therefore, depending on the power quadrant that the converter is operating, the combination between the apparent and active power flows can lead to power losses of roughly around 1 MW/0.001 pu (shaded in dark blue) to 7 MW/0.007 pu (shaded in dark red).

The Figures 20(b), 21(b), 22(b) and 23(b) compare the discrete data points retrieved by the MMC's simulation and the model proposed. As depicted, the mathematical expression presented is capable to sharply describe the semiconductor's power losses over the four power quadrants. For sake of clarity and according to the proposed model, if the converter is operating as a rectifier and

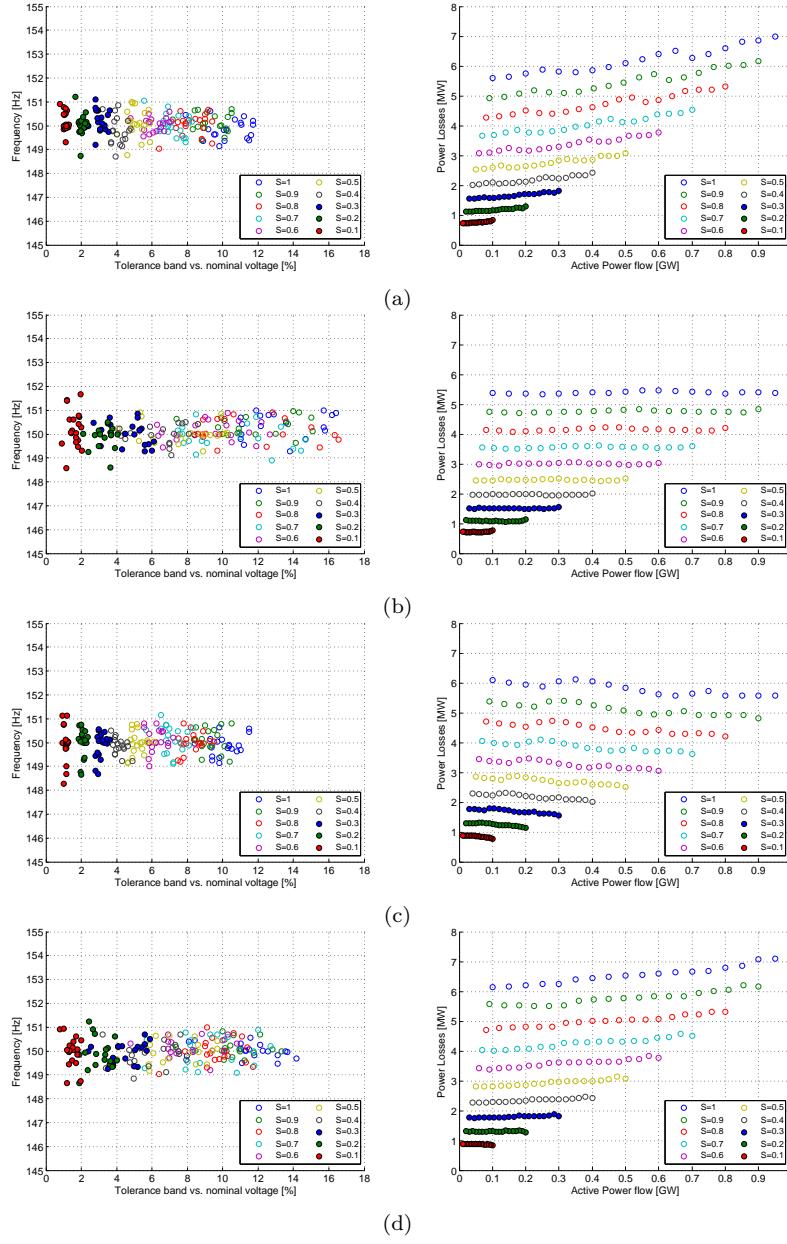


Figure 18: Semiconductor's generated losses and SMs average switching frequency for : (a) power quadrant 1 - Q1, (b) power quadrant 2 - Q2, (c) power quadrant 3 - Q3 and (d) power quadrant 4 - Q4.

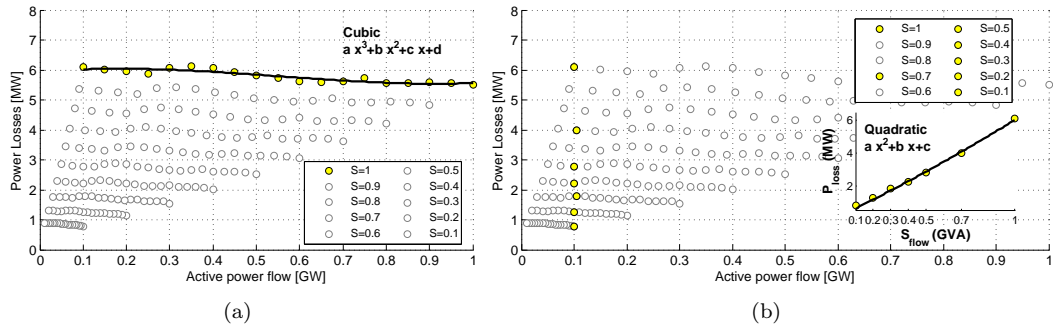


Figure 19: Illustration of the relation: (a) P_{loss} vs. P_{flow} ($S_{flow} = 1$ pu) and (b) P_{loss} vs. S_{flow} ($P_{flow} = 0.1$ pu).

Parameters		Power quadrants (see Figure 5)			
		Q1	Q2	Q3	Q4
		[pu]	[pu]	[pu]	[pu]
$P_{loss}(S_{flow}, P_{flow})$ model	a_1	1.536e-3	-6.333e-4	2.850e-3	-1.054e-3
	a_2	-5.259e-4	4.161e-4	-10.530e-3	5.022e-3
	a_3	-1.333e-3	-1.159e-4	10.200e-3	-2.899e-3
	b_1	-2.607e-3	1.515e-3	3.839e-3	-8.540e-7
	b_2	2.969e-3	-3.668e-4	-3.053e-3	-3.867e-3
	b_3	1.064e-3	-8.592e-4	-4.971e-3	2.478e-3
	c_1	-7.282e-5	-2.123e-3	-2.658e-3	-7.591e-4
	c_2	-5.397e-5	2.551e-3	4.874e-3	2.899e-3
	c_3	4.923e-4	-3.571e-4	-9.094e-4	-7.508e-4
	d_1	1.889e-3	1.752e-3	1.686e-3	2.007e-3
	d_2	3.346e-3	3.210e-3	3.738e-3	3.501e-3
	d_3	3.644e-4	3.828e-4	5.000e-4	5.251e-4
$(S_{base} = 1 \text{ GVA})$					

Table 3: Mathematical losses model of the MMC in the four power quadrants operation.

exchanging 0.5 GW/ 0.33 Gvar (inductive) from its ac grid, the converter is accordingly operating on the second power quadrant (see Figure 5). Then, the group of constants of the power quadrant 2 should be embraced to estimate the power losses generated by the MMC's semiconductors. Then, in respect to the base value depicted in the table ($S_{base} = 1 \text{ GVA}$), the power losses estimation is given by (29).

$$\left\{ \begin{array}{l} P_{flow}^{pu} = \frac{P_{flow}}{S_{base}} = 0.5 \text{ pu} \\ S_{flow}^{pu} = \frac{S_{flow}}{S_{base}} = \frac{\sqrt{P_{flow}^2 + Q_{flow}^2}}{S_{base}} = 0.6 \text{ pu} \end{array} \right. \Rightarrow \left\{ \begin{array}{l} P_{loss}(S_{flow}^{pu}, P_{flow}^{pu}) = (a_1 0.6^2 + a_2 0.6 + a_3) 0.5^3 \\ \quad + (b_1 0.6^2 + b_2 0.6 + b_3) 0.5^2 \\ \quad + (c_1 0.6^2 + c_2 0.6 + c_3) 0.5 \\ \quad + (d_1 0.6^2 + d_2 0.6 + d_3) \\ \quad = 0.003 \text{ pu} \end{array} \right. \quad (29)$$

In this view, on the presented operating conditions, the mathematical model estimates that the MMC semiconductor's are dissipating 3 MW/0.003 pu of power losses, which is corroborated in the Figure 21(b).

The accuracy of the proposed model can be validated in accordance to the individual residuals between the real and estimated points, which are presented in the Figures 20(c), 21(c), 22(c) and 23(c). Independently on the power quadrant, whenever the apparent power is higher than 0.3 GVA, the mathematical expression can estimate the power losses of the converter with a relative error up to 3%, which meticulously represents the efficiency of the converter. On the scenarios that the apparent power is not higher than 0.3 GVA, the power losses model presents an almost negligible offset to the real data set points, which increases the relative errors in this area. This occurs because for $S \leq 0.3 \text{ GVA}$ the data sets are more concentrated, particularly for $S=0.1 \text{ GVA}$, which is more difficult to reach a better closeness at these points, without compromising the model's accuracy at higher power flow's operation of the converter. Taking into account the scenario in which the model carries the highest residual, particularly $\approx 8.2 \%$ (in respect to the estimation),

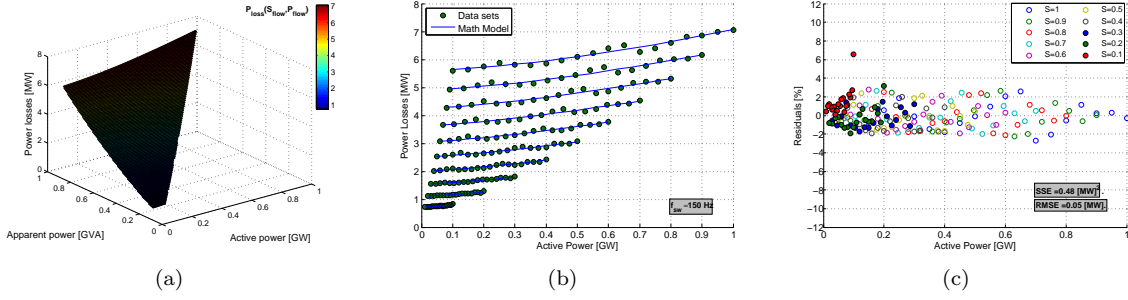


Figure 20: (a) Mathematical model of the generated losses by the MMC in the power quadrant 1; (b) $P_{loss}(S_{flow}, P_{flow})$ vs simulated data and model's domain; (c) relative error.

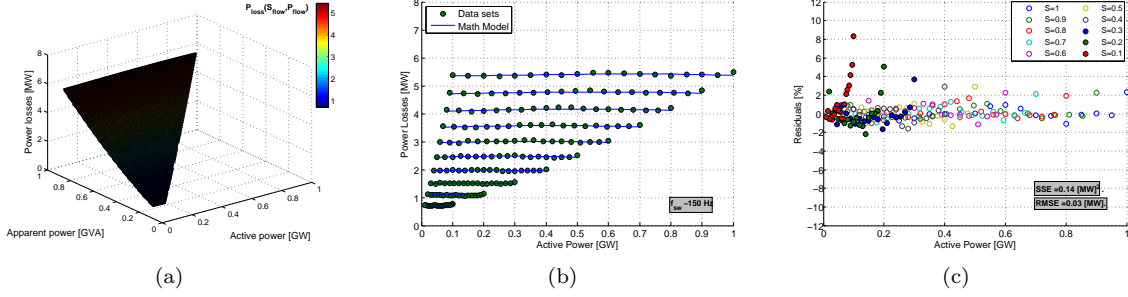


Figure 21: (a) Mathematical model of the generated losses by the MMC in the power quadrant 2; (b) $P_{loss}(S_{flow}, P_{flow})$ vs simulated data and model's domain; (c) relative error.

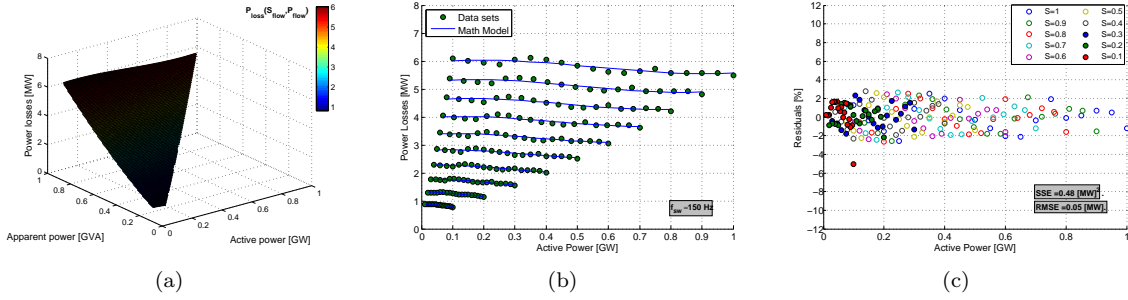


Figure 22: (a) Mathematical model of the generated losses by the MMC in the power quadrant 3; (b) $P_{loss}(S_{flow}, P_{flow})$ vs simulated data and model's domain; (c) relative error.

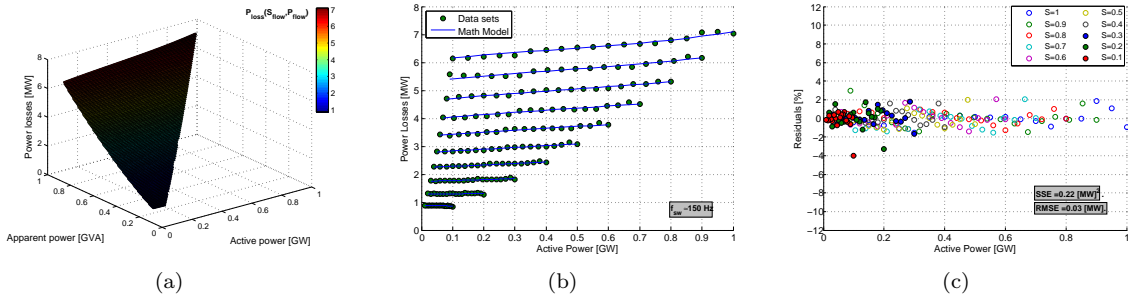


Figure 23: (a) Mathematical model of the generated losses by the MMC in the power quadrant 4; (b) $P_{loss}(S_{flow}, P_{flow})$ vs simulated data and model's domain; (c) relative error.

that occurs for the converter operation in the rectifier mode with $S=0.1$ GVA and $P=0.1$ GW (quadrant 2), the semiconductor's power losses is roughly 0.76 MW, whereas the model estimate 0.7 MW. Hence, the 8.2 % refers to a deviation of only 60 kW. Although, the deviation is relatively high, since it refers to very low power flow scenarios, under these circumstances, the relative error that characterizes the converter operation is considered to be tolerable.

5 Conclusion

In the present days, the multi-terminal HVdc grids are a viable solution to transport energy to remote and/or distant areas. The operation of such grids and their efficiency depends, among other things, on the converter terminals knowledge. This work presents a methodology that can be followed to model the semiconductor's power losses of the MMC and endorse the OPF studies with accurate models.

The power losses generated by the modular multilevel converter is strongly dependent on the system parameters used for the converter model and the methodology followed to modulate the voltages across its arms, particularly on the nature of the ZSS injected and the cell selection strategy adopted. Therefore, by electing a state of the art MMC selective control of the cells and accordingly a modern estimation method to quantify the semiconductors losses, the converter efficiency was modeled according to two operating scenarios. The active power exchange with the electrical grid, over a considerable switching frequencies range was taken into account as the first scenario. A polynomial-based expression, whose parameters were optimized according to the Levenberg-Marquardt method, was proposed to describe the converter losses generation P_{loss} when it operates between 0.1 to 1 GW (unity power factor) P_{flow} , and accordingly to the switching frequency selected f_{sw} , resulting the $P_{loss}(f_{sw}, P_{flow})$ model. Moreover, at the second stage, several combinations of $\{P, Q\}$ were considered, nonetheless, maintaining the average switching frequency of the converter cells fixed to the 150 Hz value, which accordingly to the literature is the typical switching frequency of the SMs in real applications. Then, a second polynomial-based expression was described and proposed to outline the converter efficiency over the power quadrants defined by the direction of $\{P, Q\}$. The resultant models, as presented, can accurately match the converter losses with the maximum absolute error $\leq 3\%$, which is an exceptional estimator of the power losses produced by the modular multilevel converter.

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